Constrained Maximum-Likelihood Detection for High-Speed Fiber-Optic Systems

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Abstract

In this paper, we present design techniques for constrained maximum likelihood detection (MLD), a receiver electrical signal processing technique that provides near-optimum interference compensation, yet can be implemented at Gbps data rates. Our technique determines the most likely transmitted bit given N_1 previously detected bits and N_2 received signal samples, using decision boundaries formed by (N_2-1)-dimensional planes which are implemented with comparators. We present examples of the design procedure that show that the circuitry is simple and not significantly more complex than standard detectors. Thus, the techniques are a practical method for significantly reducing the effect of chromatic and polarization dispersion, as well as interference between signals caused, e.g., by fiber nonlinearity, in Gbps lightwave systems.

1. INTRODUCTION

Maximum likelihood detection (MLD) is the optimum receiver electrical signal processing technique for interference compensation. MLD, which estimates each transmitted bit from *multiple* received signal samples, can provide significant improvement over techniques based on symbol-by-symbol detection. Specifically, it significantly reduces the effect of intersymbol interference due to chromatic and polarization dispersion in optical fibers, as well as interference between signals in a wavelength division multiplexed system, e.g., interference due to fiber nonlinearity. However, at the Gbps data rates of high-speed fiber-optic systems, MLD is far too complicated to be performed at reasonable cost with today's technology. Therefore, in order for the potential of MLD to be realized, techniques must be devised that are practical at Gbps data rates, yet approach the performance of MLD.

Previous papers (e.g., [1,2,3,4]) have studied the reduction of intersymbol interference (ISI) in lightwave systems with electrical signal processing at the receiver. Receiver signal processing has the advantage that it improves performance without modifying the transmitted signal and can be adaptive to changing source or channel conditions. The simplest technique, a tapped-delay-line linear equalizer, compensates only for linear ISI, such as polarization dispersion [3] and chromatic dispersion in coherent detection systems [4]. Although it is easy to implement at Gbps data rates, this equalizer requires a larger area than a single integrated circuit (IC), because analog delays require distances of several inches. A better technique is nonlinear cancellation (NLC), which can compensate for both linear and nonlinear ISI (such as from chromatic dispersion in direct detection systems) from previously detected bits. Moreover, NLC can be implemented on the detector IC at Gbps data rates [5]. However, it cannot compensate for nonlinear ISI from bits that haven't yet been detected, i.e., precursor nonlinear ISI. The optimum receiver signal processing technique, MLD, determines the most likely transmitted bit from multiple received signal samples, as compared to the previously mentioned symbol-by-symbol detection schemes. It was shown in [1] that in many cases MLD is significantly better than linear equalization or NLC, allowing for reliable detection even when the received signal eye is closed. However, MLD requires analog multipliers and analog storage over many symbols, making implementation impractical at Gbps data rates.

In this paper, we show how to approximate MLD with lower complexity circuitry, using threshold detectors and digital logic which can be implemented on the detector IC. To reduce complexity, we constrain the number of symbol periods for MLD, considering MLD of the transmitted bits given N_1 previously detected bits and N_2 received signal samples. Thus, ISI from previously detected bits is removed by decision feedback [5,6,7], and the receive signal space is reduced to N_2-dimensional. The optimal decision regions over the N_2-dimensional receiver space are then approximately defined using (N_2-1)-dimensional planes perpendicular to the axes - these planes are implemented by comparators, with the detected bits determined by simple combinatorial logic. We present a general design procedure for the technique, which involves circuit complexity versus performance tradeoffs. We use two examples to illustrate the design procedure and the tradeoffs, showing application to coherent and direct detection systems with polarization and chromatic dispersion, as well as systems with nonlinearities. Results show that the performance of these techniques approaches that of MLD.

In Section II, we briefly describe maximum likelihood detection, outline the assumptions under which it provides

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optimal detection, and we describe a general design procedure for our technique. In Section III, we illustrate the procedure for two applications. A summary and conclusions are presented in Section IV.

2. MAXIMUM LIKELIHOOD DETECTION

Let us first consider a received signal corrupted by ISI and additive white Gaussian noise, which, e.g., could be due to polarization dispersion or chromatic dispersion in a *coherent* detection system. For on-off keying, the received electrical signal sample at time t_k is given by

$$r_k = s_k + n_k = x_k + \sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty} a_l x_{k-l} + n_k \qquad (1)$$

where x_k is the transmitted signal (0,1), s_k is the received signal with ISI, and n_k is the noise. Note that finite channel memory will truncate the sum in Eq. (1). We assume "0"'s and "1"'s are equiprobable at the channel input. Optimal detection (MLD) in the presence of additive white Gaussian noise requires finding the input data sequence that would produce the noise-free output sequence (unquantized) *closest* to the received discrete-time signal sequence actually received. Closeness here is defined in terms of Euclidean distance measured at the channel output. The above definition of MLD would require reception of the whole data stream before any detection decisions are made. In practice, detection decisions are typically made after examining a sliding window on the sequence. The length of the sliding window is typically six to seven times the constraint length of the channel memory, and this achieves performance that is close to MLD [8]. The error performance of MLD, in the high signal-to-noise ratio regime, is accurately reflected by the minimum Euclidean distance between received signal vectors. We compute the minimum Euclidean distance for a channel, and use this as a benchmark to evaluate the techniques developed in this paper. Elegant techniques have been used to cast MLD as a dynamic programming problem; the most famous of these is the Viterbi algorithm [8]. Although the Viterbi algorithm dramatically reduces the computational burden of MLD, it requires

- Soft decisions and multiplications to determine the state metrics: i.e., the channel output must quantized to multiple bits to utilize the algorithm effectively.
- Storage of these metrics over 6 to 7 times the duration of the ISI.

Neither of the two items are practical at Gbps data rates with current technology.

Therefore, we consider two approximations to MLD - one to reduce the number of state metrics and the second to replace the soft decisions, multiplications, and additions by comparators and digital logic[1]. First, the number of states in the detector can be reduced by using a sliding window technique with decision feedback [1,6,7]. Specifically, with a window of N bits, N_1 previously detected bits are used to determine the state (i.e., one of the 2^{N_1} possible cases that exist prior to detection of the current bit), and N_2 signal samples are used to determine the detected bit ($N=N_1+N_2$). The detector calculates the Euclidean distance between the received signal vector of length N_2 and each of the 2^{N_2} stored signal vectors (symbol sequences) to determine the stored signal vector that is closest to the received signal vector and outputs the bit corresponding to the first bit in that stored signal vector. There is a separate set of 2^{N_2} stored signal vectors for each of the possible 2^{N_1} states, for a total of $2^{N_1+N_2}$ (or 2^N) signal vectors.

Finding the closest signal vector requires computing Euclidean distances, and computing Euclidean distance in $N_2>1$ dimensional space requires analog-to-digital (A/D) conversion and multiplication. To avoid this, we first partition the receive signal space into subdivisions associated with each input sequence, labeling each subdivision with a "0" or a "1" depending on the bit to be detected in that sequence. The partitioning and association is done to ensure that any received signal point in a partitioned region is closest to the data sequence associated with that region. Note that all the subdivisions associated with a given bit may or may not form disjoint decision regions. Thus, MLD of the transmitted bit can be done by determining which region the received signal point is in, i.e., by determining the location of the received signal point relative to the decision boundaries between the regions. Of course, determining this location also requires multiplications.

However, because fiber-optic systems typically operate with extremely low bit error rates, the error performance is mainly dependent on the effective minimum distance of the detection system. That is, the performance of the sliding window detector can be determined from the *minimum* Euclidean distance between received signal vectors with the same N_1 previously detected bits and different first bits, followed by any combination of N_2-1 bits not yet detected, i.e., [1]

$$d_{\min} = \min_{\substack{k,i \\ x_k \neq x_i \\ \{x_{k-N_1}\cdots x_{k-1}\} = \{x_{i-N_1}\cdots x_{i-1}\}}} \left[\sum_{j=0}^{N_2} (s_{k-j} - s_{i-j})^2\right]^{1/2} . \qquad (2)$$

Specific results are given in [1][2]. Note that in an optical system, the optical power penalty is $10\log_{10}(d_{\min}/d_{\min 0})$, where $d_{\min 0}$ is the minimum Euclidean distance without

1. Note that since we are not using the Viterbi algorithm, our approach applies to nonlinear as well as linear ISI.

interference.

Therefore, the performance of MLD is mainly determined by short segments of the decision boundary that are $d_{min}/2$ away from points in each decision region. We refer to these segments as the critical segments of the decision boundary. Thus, we can closely approximate the performance of MLD with decision boundaries defined by planes that closely approximate these critical segments only, while maintaining at least $d_{min}/2$ from all points in the two regions. The advantage of using planes to approximate the decision boundaries is that a plane perpendicular to an axis in the receive signal space can be implemented by a comparator operating over the time slot corresponding to this axis. Outputs of comparators operating over multiple time slots can be combined using digital logic to approximate a decision boundary to any degree of accuracy. Note that the comparators and digital logic can be integrated into the detector IC. Moreover, the receive signal space can be rotated by combining the weighted (by a fixed amount) signals in different time slots, thereby allowing a comparator to generate a plane at any angle to the axes. This combining of analog signals requires a tapped delay line, however, which cannot be integrated into the detector IC. By using this technique, we can approximate the performance of MLD with circuitry that is practical at Gbps data rates, i.e., can operate at the maximum data rate of a single threshold detector, and trade off circuit complexity for improved performance.

This leads us to the following design procedure (note that we assume that the ISI is known (or at least the type of the ISI is known)):

1. Choose a window size (N_1 and N_2).
2. Plot the N_2-dimensional receive signal space and optimum decision boundaries.
3. Choose the number of comparators to approximate the decision boundaries and, if needed, the rotation.
4. Determine the optimum location of the planes to approximate the decision boundaries.
5. Design the circuitry.

Note that a separate design and analysis procedure is required for each type of ISI, and the design and performance will vary with N_1, N_2, and the comparator approximation.

By our definition of MLD given N_1 and N_2 constraints, standard threshold detection is just constrained MLD with $N_1=0$ and $N_2=1$, while NLC is constrained MLD with $N_1>0$ and $N_2=1$. In this paper, we are concerned with MLD using multiple signal samples, i.e., MLD with $N_2>1$ ($N_1\geq 0$).

Below we give two examples for the design procedure and study the performance of the techniques. Example 1 studies the simplest case - each bit interferes with the preceding bit - which, although simple, is equalized very poorly by NLC. We discuss the design tradeoffs of the number of symbols and comparators and of receive signal space rotation. The second example shows how MLD can be used with co-channel interference.

3. EXAMPLES

3.1 Example 1

Consider linear ISI due to each bit interfering with the previous bit, i.e.,

$$s_k = x_k + \alpha x_{k+1} \quad , \quad \alpha<1 \quad . \tag{3}$$

This could be due to polarization dispersion in a direct or coherent detection system, chromatic dispersion in a coherent detection system, or nonideal receiver response [1]. Figure 1 shows the 2-dimensional receive signal space with this type of ISI, for an example case of $\alpha=0.5$. The bit patterns that generate each point in the receive signal space are shown, with the bit to be detected underlined.

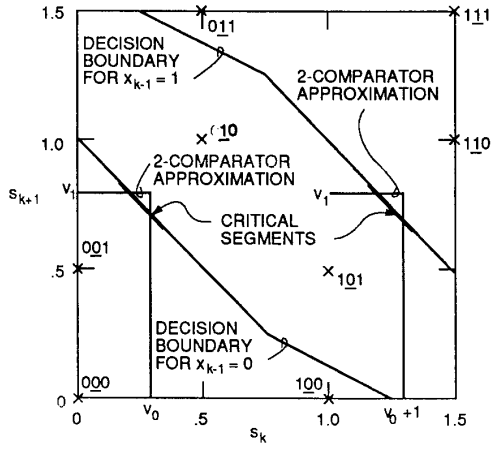

Figure 1 Receive signal space with ISI from the next bit, showing the optimum decision boundaries and a two comparator approximation to the critical segments of these boundaries.

For standard threshold detection with a single comparator (MLD with $N_1=0, N_2=1$), the optimum threshold V_0 is

$$V_0 = (1+\alpha)/2 \quad , \tag{4}$$

2. These results assume that the previous bits have been detected correctly. Whereas this assumption is not entirely correct, MLD does significantly improve performance in spite of occasional (though rare) errors in the feedback. This issue of errors in the feedback has been addressed by others [9,10], and we will not dwell on it any further.

and

$$d_{\min} = (1-\alpha) \quad . \tag{5}$$

For the range $0 \le \alpha \le .5$, NLC (MLD with $N_1=1$, $N_2=1$)[3] does not change the optimum threshold and hence offers no improvement in performance. This is because the ISI is due to bits that haven't yet been through the detection process. However, for $.5 \le \alpha \le 1$, NLC can improve performance if we determine x_k from s_{k-1}, i.e., the signal sample in the time slot before the bit to be detected.[4] Specifically, let

$$\hat{x}_k = \mathrm{sgn}(s_{k-1}-V_0) \tag{6}$$

where the hat denotes the estimate of the detected bit[5], with

$$V_0 = \begin{cases} \alpha/2 \ , & \text{if } x_{k-1}=0 \\ 1+\alpha/2 \ , & \text{if } x_{k-1}=1 \end{cases} \quad . \tag{7}$$

Thus, for NLC,

$$d_{\min} = \begin{cases} 1-\alpha \ , & \text{if } 0 \le \alpha \le .5 \\ \alpha \ , & \text{if } .5 < \alpha \le 1 \end{cases} \quad . \tag{8}$$

To illustrate our design procedure for constrained MLD, for step 1, let $N_1=1$ and $N_2=2$. For step 2, the signal points and optimum decision boundaries are also shown in Figure 1. Note that there are $2^{N_1} = 2$ decision boundaries, one for when the previous bit is "0" ($x_{k-1} = 0$), and one for $x_{k-1} = 1$. It can easily be seen from this figure that

$$d_{\min} = \sqrt{(1-\alpha)^2+\alpha^2} \quad , \tag{9}$$

with the critical segment of each boundary that determines the receiver performance (because it is $d_{\min}/2$ from points in each decision region) also shown in Figure 1. For step 3, with no multipliers, we approximate the critical segment of each boundary with two comparators, i.e., lines perpendicular to the s_k and s_{k+1} axes, as shown in Figure 1. Considering the approximation to the decision boundary for $x_{k-1}=0$, the optimum location of the lines, i.e., comparator thresholds V_0 and V_1, are determined by shifting these lines until they are the maximum distance from points 010 and 001. For $1/3 \le \alpha \le 2/3$, this occurs when

$$\alpha - V_0 = 1 - V_1 = \sqrt{V_0^2+(V_1-\alpha)^2} \quad , \tag{10}$$

or,

$$V_0 = \alpha/2+\Delta \tag{11}$$

$$V_1 = 1-\alpha/2+\Delta \tag{12}$$

where

$$\Delta = 1-\alpha/2-\sqrt{2\alpha(1-\alpha)} \quad , \tag{13}$$

and

$$d_{\min} = 2(1-\sqrt{2\alpha(1-\alpha)}) \quad . \tag{14}$$

For α outside this range, a two comparator approximation is not useful. Specifically, the optimum threshold values are

$$V_0 = \begin{cases} -\infty \ , & \text{if } 0 \le \alpha \le 1/3 \\ \alpha/2 \ , & \text{if } 2/3 \le \alpha \le 1 \end{cases} \qquad V_1 = \begin{cases} 1+\alpha/2 \ , & \text{if } 0 \le \alpha \le 1/3 \\ -\infty \ , & \text{if } 2/3 \le \alpha \le 1 \end{cases} \tag{15}$$

and $d_{\min}$ is given by Eq. (8). The approximation to the decision boundary for $x_{k-1}=1$ is the same as that given above, except that V_0 is increased by 1.

For step 5, we first note that although 2 comparators are required for each boundary approximation, V_1 is the same for both the $x_{k-1}=0$ and $x_{k-1}=1$ boundaries, and thus a total of only 3 comparators (rather than 4) are required. Figure 2 shows the circuitry required to implement this MLD approximation, with a multiplexer used to choose the decision boundary and AND gates used to define decision regions from the line segments.

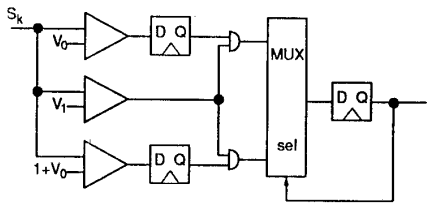

Figure 2 Circuitry for the two comparator approximation of MLD with $N_1=1$ and $N_2=2$ for ISI from the next bit.

Note that we have avoided analog feedback by using multiple comparators per time slot as in [5] for NLC. At lower speeds we could eliminate the multiplexer and a comparator by adjusting V_0 ($1+V_0$) based on the previously detected bit.

Figure 3 compares $d_{\min}$ for this (2-comparator approximation of MLD with $N_2=2$) detector to that for a standard detector, NLC, and MLD with $N_1=1$ and $N_2=2$. For unconstrained MLD, it can easily be shown that

$$d_{\min} = \sqrt{1+\alpha^2} \quad . \tag{16}$$

The performance of unconstrained MLD is also shown in Figure 3. At the minimum value (over α) of $d_{\min}$, the 2-

3. With this type of ISI, the NLC performance is not increased with $N_1>1$, for $.5 \le \alpha \le 1$, and $N_1>0$, for $0 \le \alpha \le .5$.

4. Note that this is the only case in this paper where we consider using signal samples from slots before that of the bit to be detected.

5. In the rest of the paper we assume (nearly) error free detection, i.e., $\hat{x}_k = x_k$.

comparator approximation has a 17% improvement in d_{min} (0.7 dB lower optical power penalty) over NLC, but is 0.8 dB higher than constrained (N_2=2) MLD and 2.3 dB higher than unconstrained MLD. Below we describe methods for improving performance and approaching the performance of unconstrained MLD through increased circuit complexity.

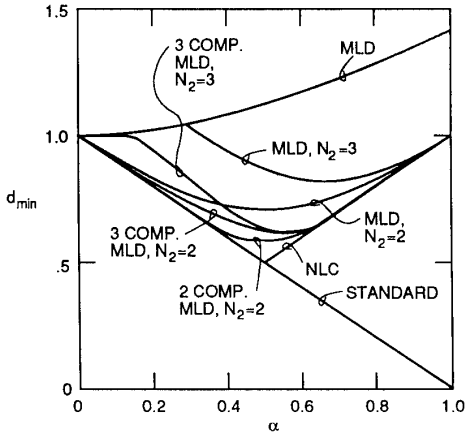

Figure 3 d_{min} for various detectors with ISI from the next bit.

3.1.1 Ways to Improve Performance We first note that the above technique is not the only way to approximate the decision boundary by two comparators. The boundary can also be approximated by two comparators with the 1/4 plane of Figure 1 facing the upper right corner rather than the lower left as shown in the figure. However, although the threshold values and logic for this approximation are different from Eqns. (11,12) and Figure 2, the performance and circuit complexity is unchanged.

We can improve performance (at the cost of increased circuit complexity) by using more lines to approximate the decision boundary. For example, using a 3-comparator approximation which requires an additional comparator, the performance is improved by about 6%, as shown in Figure 3.

In addition, we can also improve performance by rotating the receive signal space. Note that the critical segments of the optimum decision boundaries in Figure 1 are straight lines at angle $90°+\tan^{-1}\left[\frac{1-\alpha}{\alpha}\right]$. A detector with such decision boundaries has the same d_{min} as constrained (N_2=2) MLD, Eq. (9), and thus approaches the performance of constrained MLD at low bit error rates. These straight line boundaries can be obtained by rotating the receive signal space by $\theta=\tan^{-1}\left[\frac{1-\alpha}{\alpha}\right]$ with a tapped delay line and using two comparators with the appropriate thresholds.

Another method for improvement is to increase N, which can be accomplished by increasing N_1 and/or N_2. For Example 1, increasing N_1 does not increase performance, since the receive signal points do not depend on the bits before x_{k-1}. However, increasing N_2 does improve performance, at the expense of increased circuit complexity. For N_2=3, the receive signal space is 3-dimensional, and with the appropriate decision boundaries, the performance of the resulting circuitry with a 3 comparator approximation is as shown in Figure 3.

3.2 Example 2

Consider the transmission of two on-off keyed signals at different frequencies through an optical fiber with a peak power limitation P and direct detection at the receiver. Such a power limitation could be due to a semiconductor amplifier or fiber nonlinearity. Thus, when a "1" is transmitted at one frequency and a "0" is transmitted at the other, the "1" has an optical power (electrical current) of P, while, if "1"'s are transmitted at both frequencies, each signal has an optical power of $P/2$. Figure 4 shows the 2-dimensional receive signal space for this case.

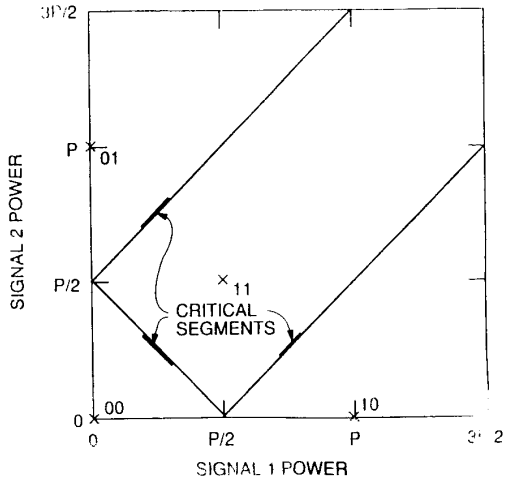

Figure 4 Receive signal space for two signals with peak total power limitation showing the optimum decision boundaries and a two comparator approximation to the critical segments of these boundaries.

With standard (one-dimensional) detection, the optimum decision threshold is $P/4$, i.e., $d_{min}=P/2$ and there is a 3 dB optical (6 dB electrical) power penalty due to the power limitation. However, since the signal coordinates are correlated, performance will be improved by joint detection of the signals. Specifically, if the two-dimensional receive

signal space is used by the detector with the optimum decision boundaries as shown in Figure 4 (i.e., two-dimensional MLD),

$$d_{\min} = \sqrt{2}P/2 \quad , \tag{17}$$

i.e., the optical power penalty is only 1.5 dB (3 dB electrical penalty). Note that 2-dimensional MLD is unconstrained MLD in this example.

To implement such a detector, note that if we rotate the receive signal space 45°, all three critical segments of the optimum decision boundary (see Figure 4) are vertical or horizontal lines, i.e., the decision boundary can be implemented by comparators with thresholds at $\pm V_0 = \pm\sqrt{2}P/2$. Figure 5 shows the circuit design[6], which has the two-dimensional (unconstrained) MLD optical power penalty of only 1.5 dB (at low bit error rates), using only one more comparator than standard detection of two signals.

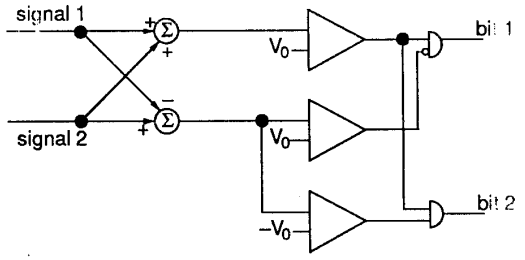

Figure 5 Circuitry for the rotation approximation of MLD for two signals with peak total power limitation.

4. CONCLUSIONS

In this paper, we have presented design techniques for constrained MLD, a receiver electrical signal processing technique that provides near-optimum interference compensation, yet can be implemented at Gbps data rates. Our technique determines the most likely transmitted bit given N_1 previously detected bits and N_2 received signal samples, using decision boundaries formed by (N_2-1)-dimensional planes which are implemented with comparators. We presented two examples that demonstrated the design procedure and the tradeoff of circuit complexity versus performance. These examples showed that the circuitry is simple and not significantly more complex than standard detectors. The examples also showed that these techniques can significantly reduce the optical power penalty due to interference. In summary, by using multiple detectors with digital logic, we can implement an approximation to MLD that compensates for interference almost optimally in Gbps data rate lightwave systems. Specifically, the techniques are a practical method for significantly reducing the effect of chromatic and polarization dispersion in long-haul and undersea lightwave systems, as well as reducing the effect of interference between signals caused by fiber nonlinearity in wavelength division multiplexed undersea lightwave systems.

6. Note that since sin45°=cos45°, signal weighting before combining is not required.

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